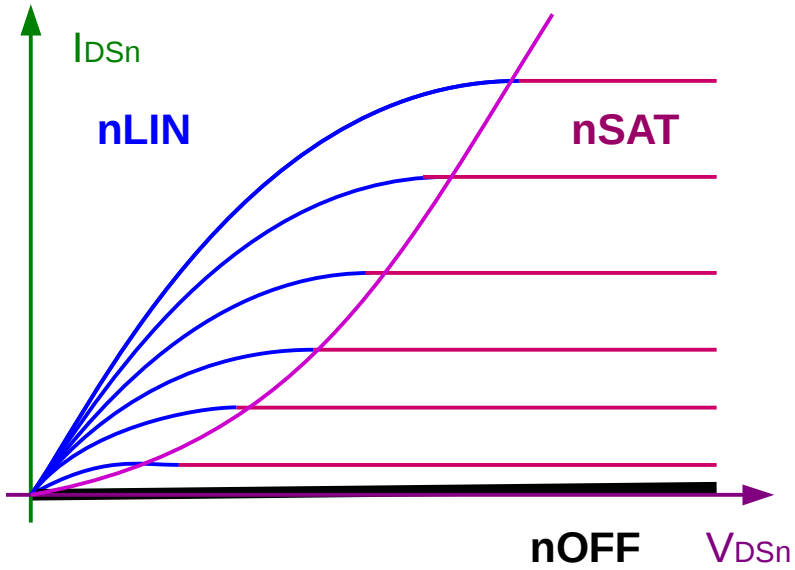
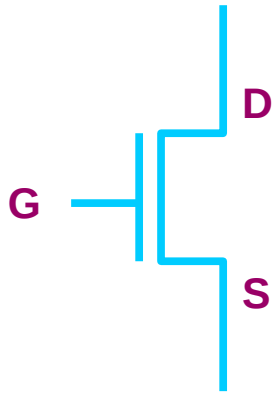
CMOS Inverter

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Operation Modes



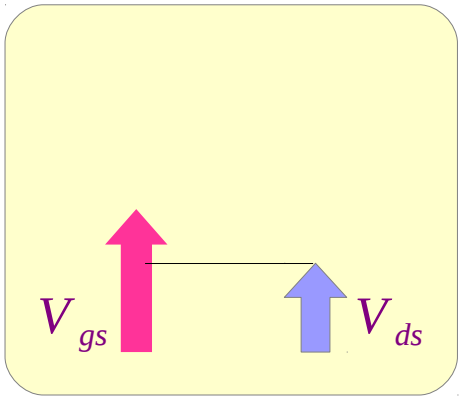


nLIN $I_{ds} \propto V_{ds}$

nSAT $I_{ds} = const$

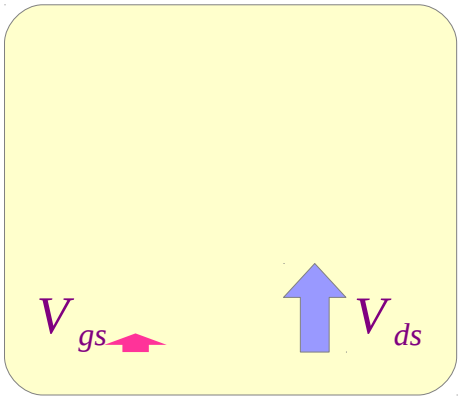
nOFF $I_{ds} = 0$

Operation Modes and Bias Voltages



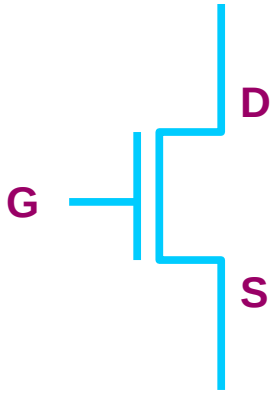
$I_{ds} \propto V_{ds}$

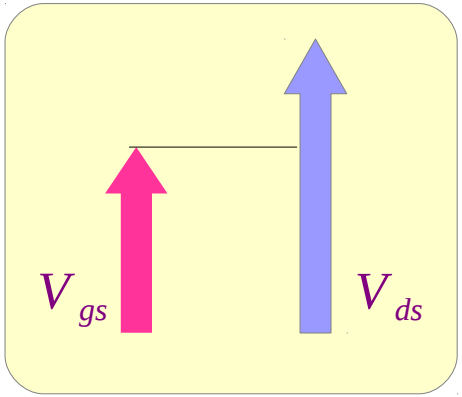
nLIN



$I_{ds} = 0$

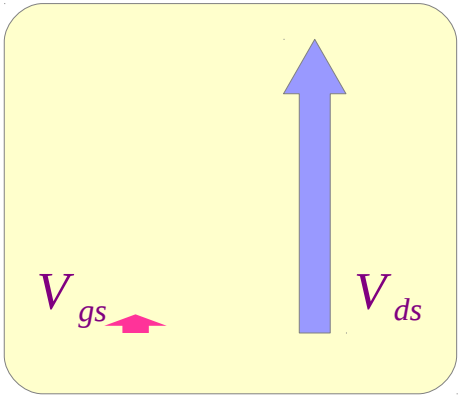
nOFF





$I_{ds} = c$

nSAT

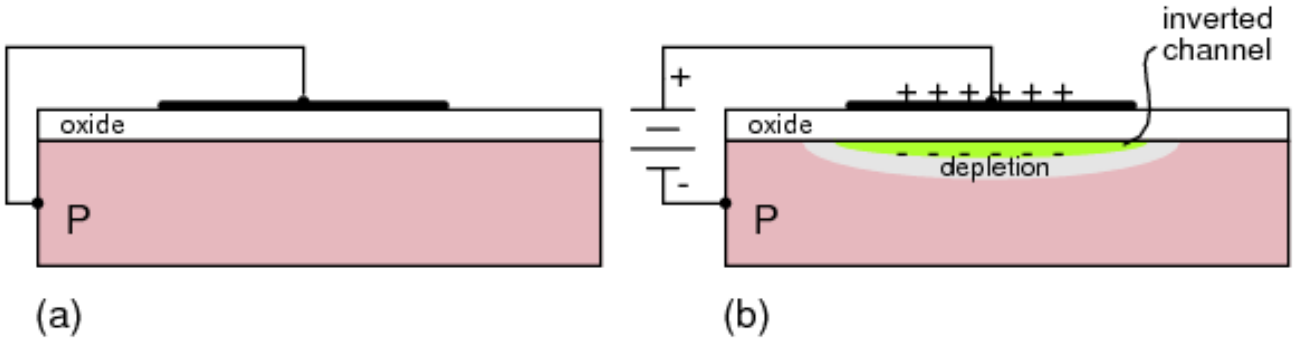


$I_{ds} = 0$

nOFF

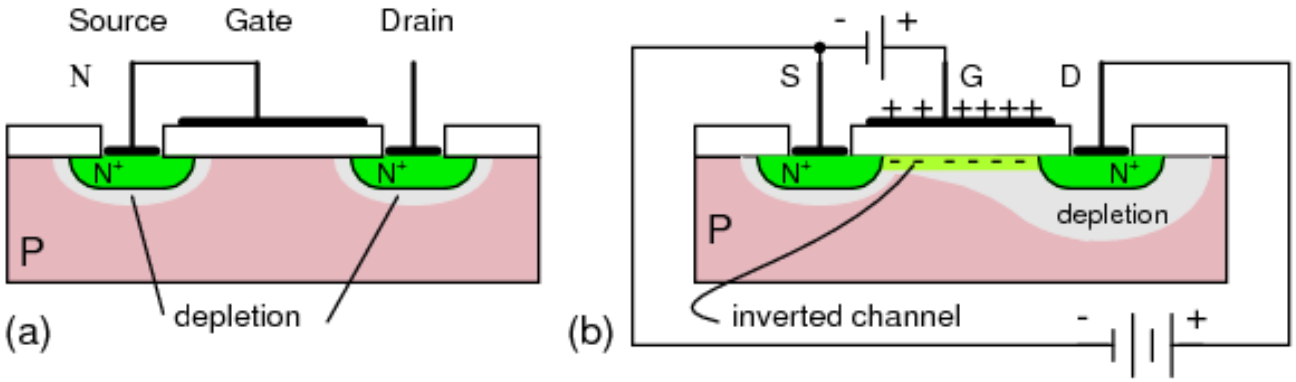
nMOS Bias

https://en.wikipedia.org/wiki/CMOS



N-channel MOS capacitor: (a) no charge, (b) charged.

nOFF

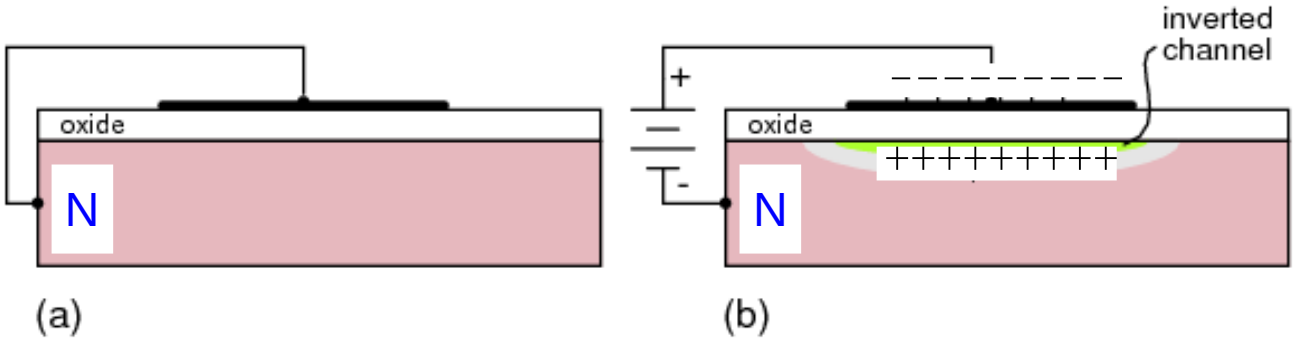


nLIN

N-channel MOSFET (enhancement type): (a) 0 V gate bias, (b) positive gate bias.

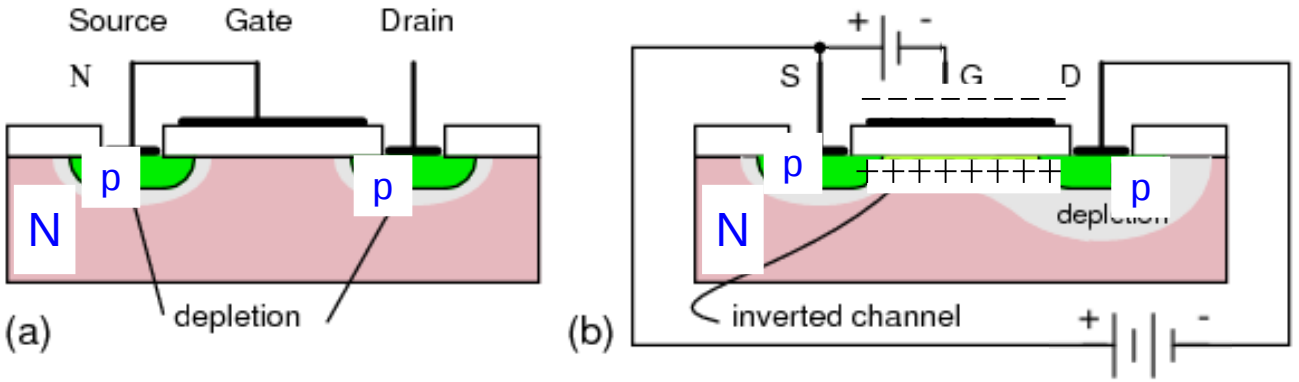
pMOS Bias

https://en.wikipedia.org/wiki/CMOS



N-channel MOS capacitor: (a) no charge, (b) charged.

pOFF

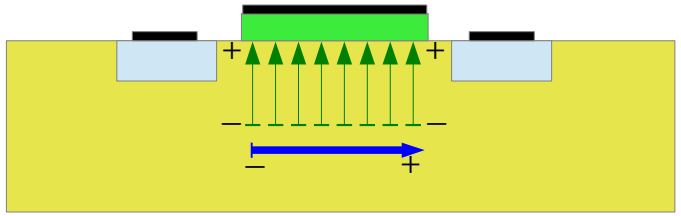


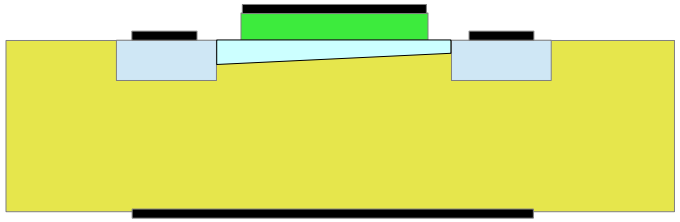
pLIN

N-channel MOSFET (enhancement type): (a) 0 V gate bias, (b) positive gate bias.

Pinch-Off

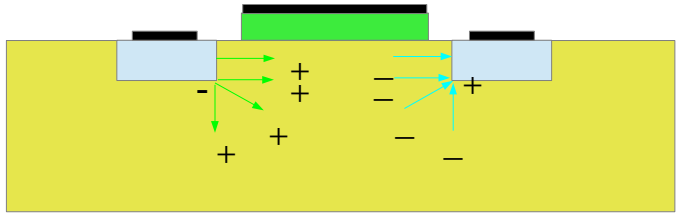
https://en.wikipedia.org/wiki/CMOS



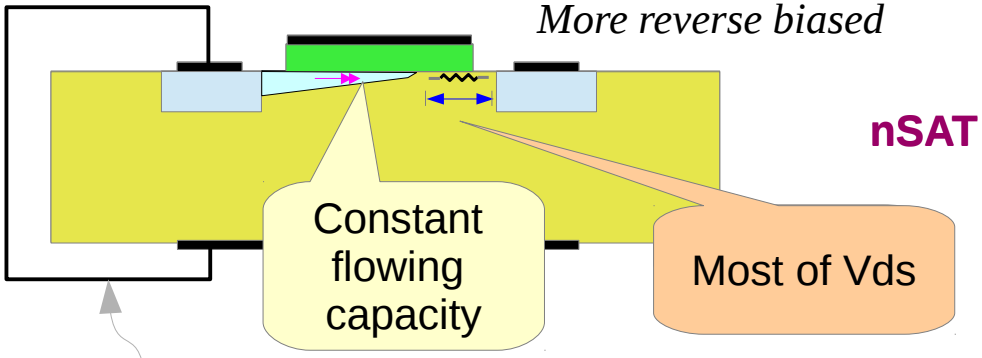


nLIN

More reverse biased



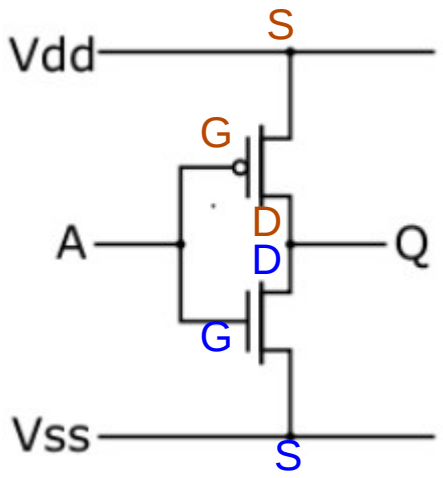
More reverse biased

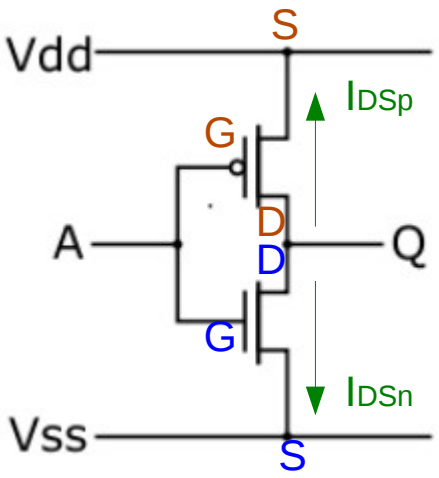


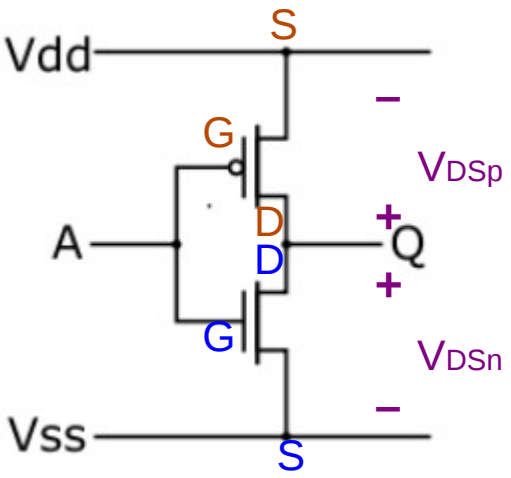
nSAT

To prevent forward
biased junction

Notation







Current Notation

Voltage Notation

$$V_{in} = V_{GSp} + V_{dd} = V_{GSn}$$

$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

https://en.wikipedia.org/wiki/CMOS

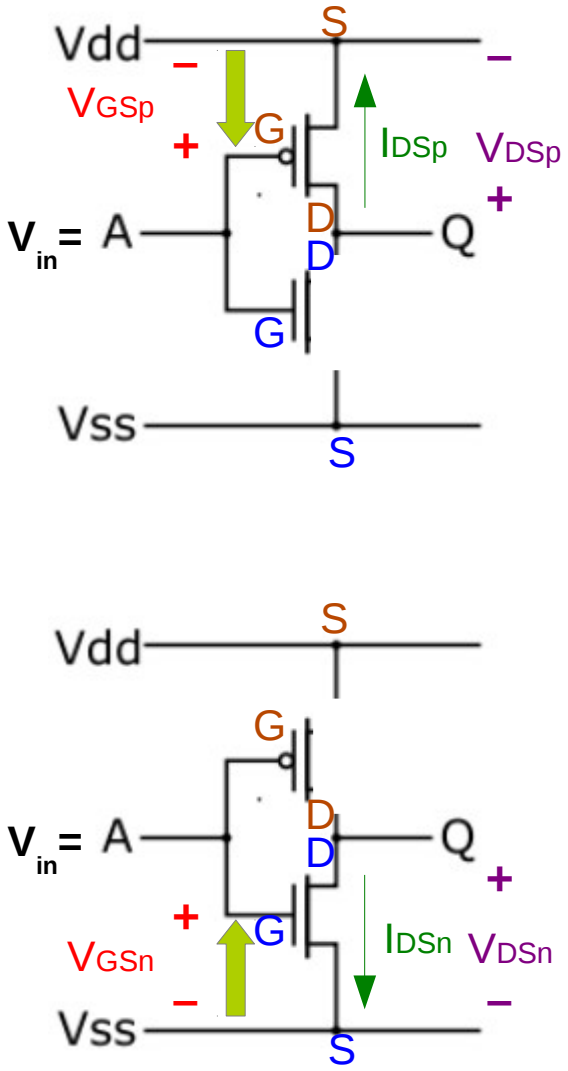
Input Voltage

$$V_{GSp} = V_{Gp} - V_{Sp}$$
$$= V_{in} - V_{dd}$$

$$V_{SGp} = V_{Sp} - V_{Gp}$$
$$= V_{dd} - V_{in}$$

$$V_{in} = V_{GSp} + V_{dd}$$
$$= V_{GSn}$$

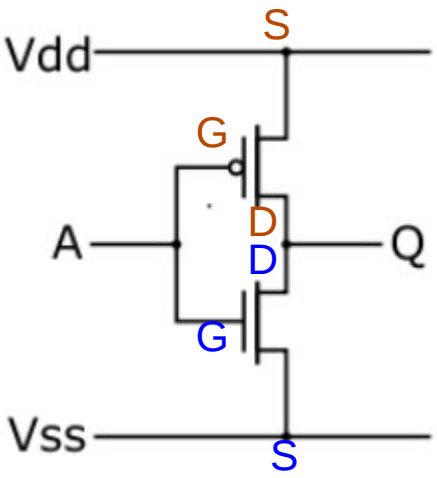
$$V_{GSn} = V_{Gn} - V_{Sn}$$
$$= V_{in} - V_{ss}$$

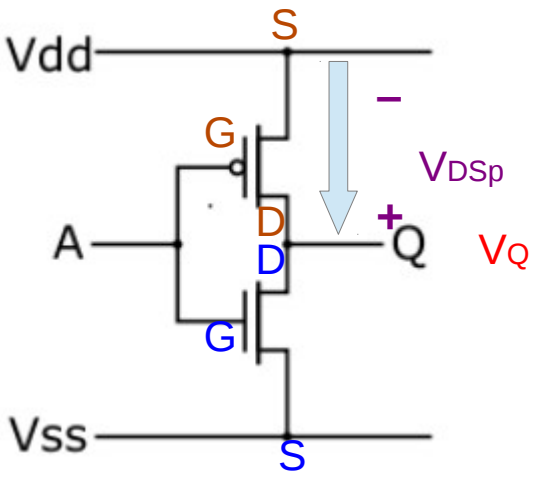


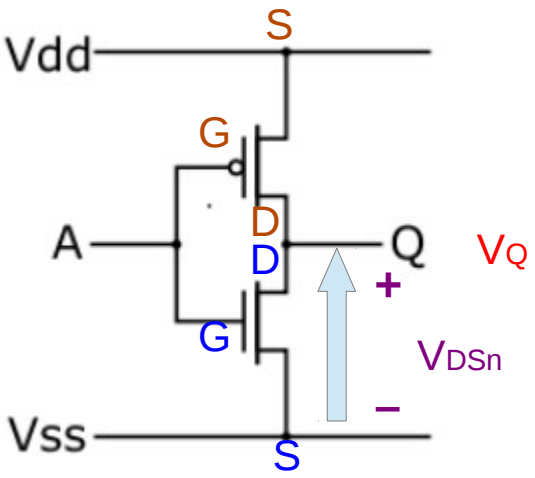
https://en.wikipedia.org/wiki/CMOS

Output Voltage

https://en.wikipedia.org/wiki/CMOS







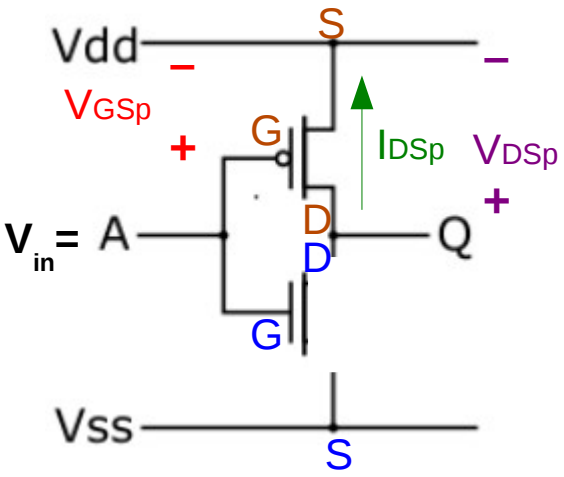
$$V_Q = V_{DSp} + V_{Sp} = V_{DSp} + V_{dd}$$

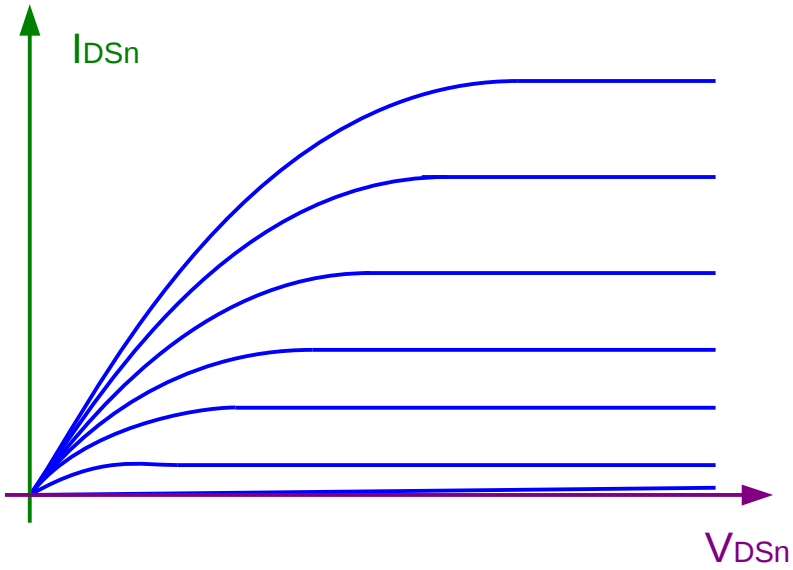
$$V_Q = V_{DSn} + V_S = V_{DSn} + V_{ss} = V_{DSn}$$

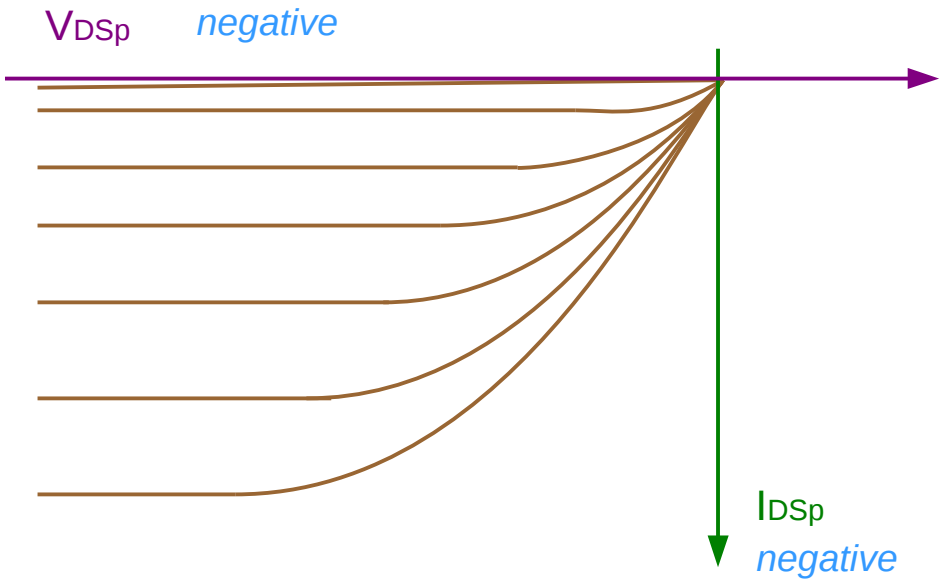
$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

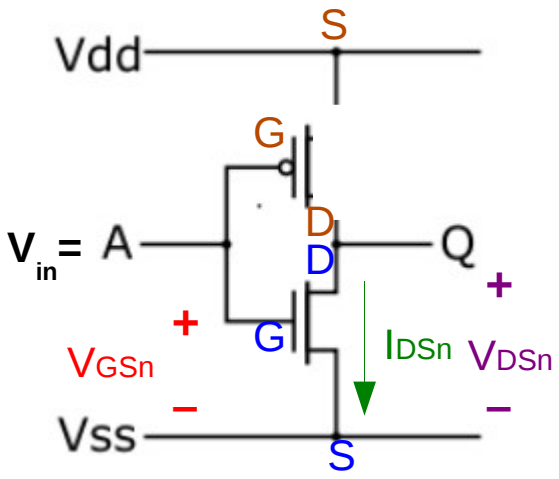
Characteristic Curves

https://en.wikipedia.org/wiki/CMOS



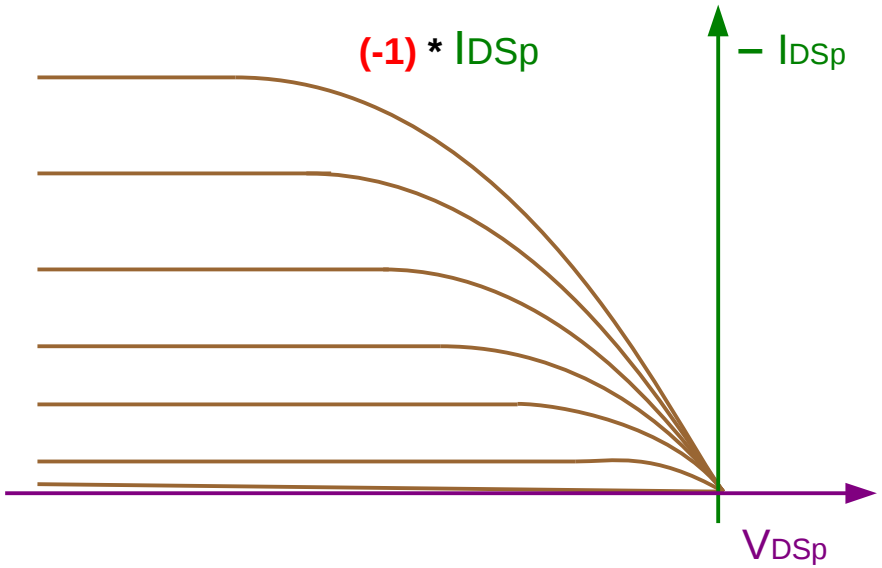


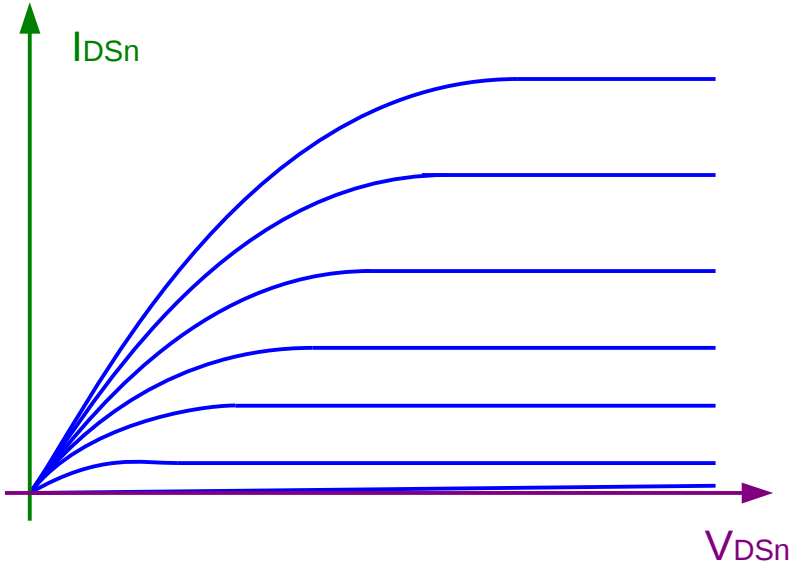


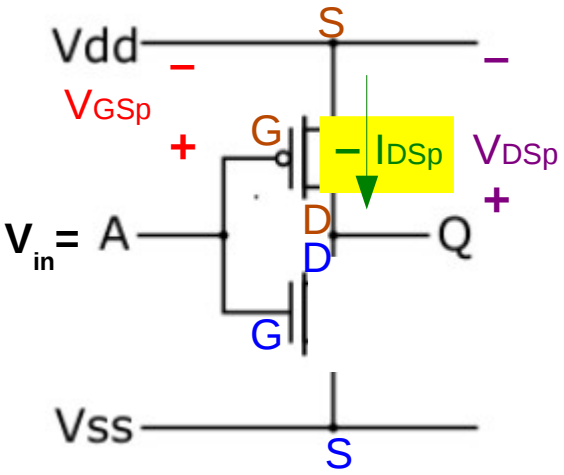


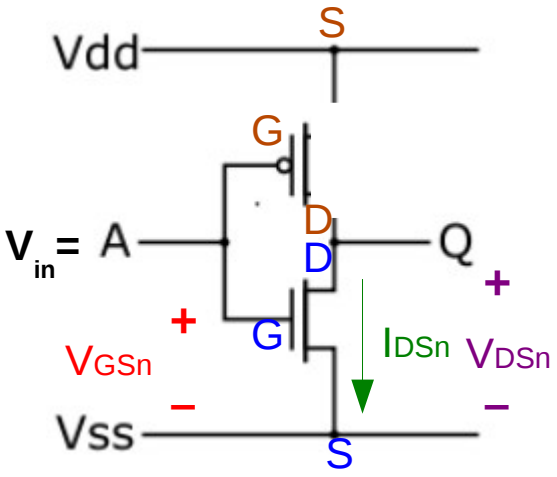
Flip up pMOS curves

https://en.wikipedia.org/wiki/CMOS



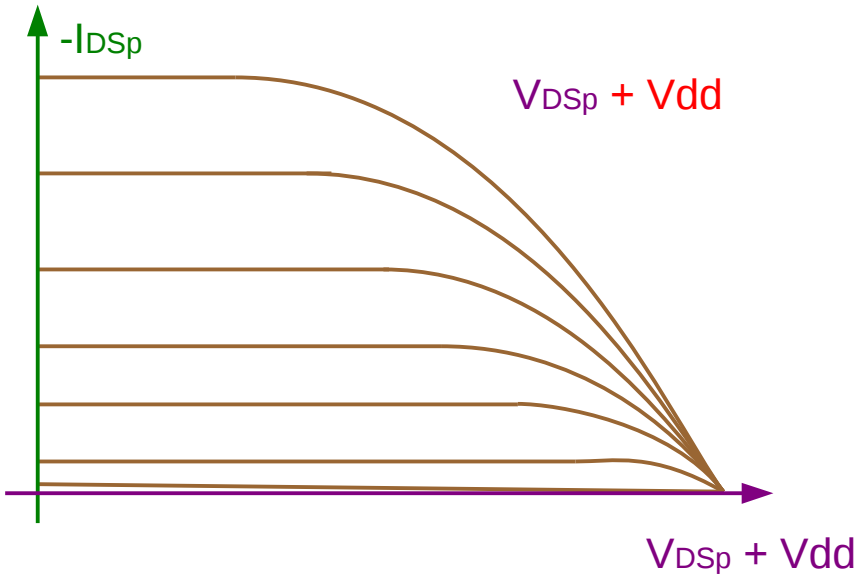


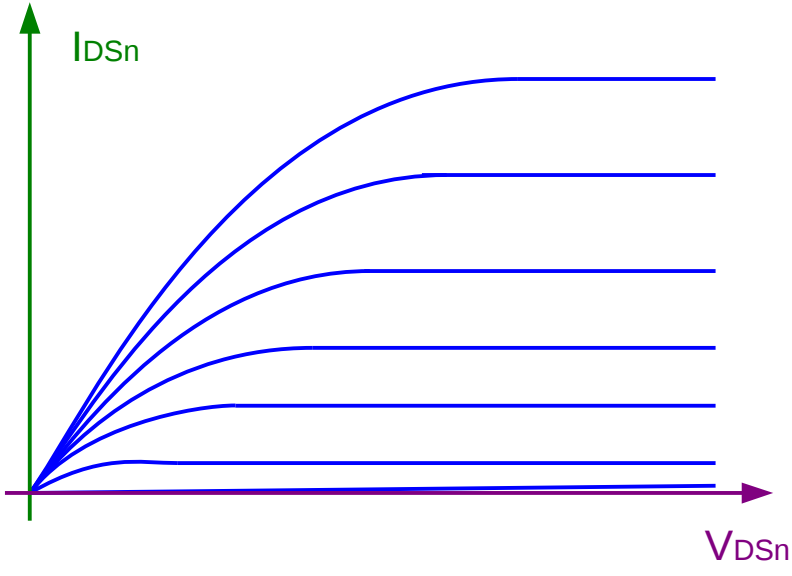


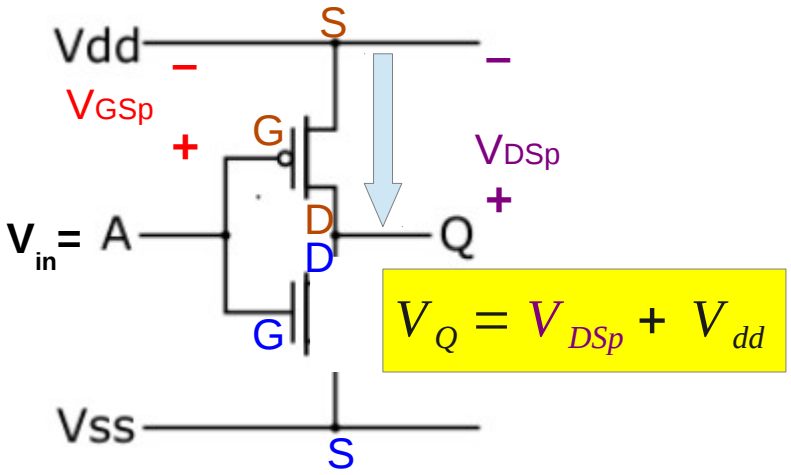


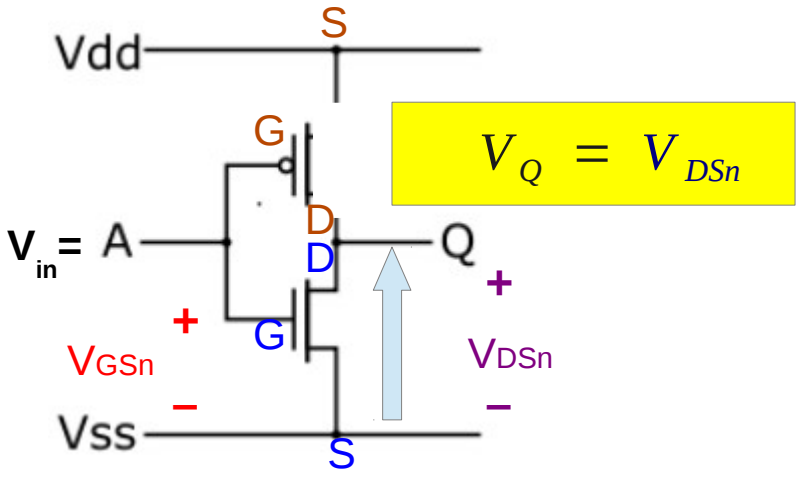
Shift right pMOS curves

https://en.wikipedia.org/wiki/CMOS







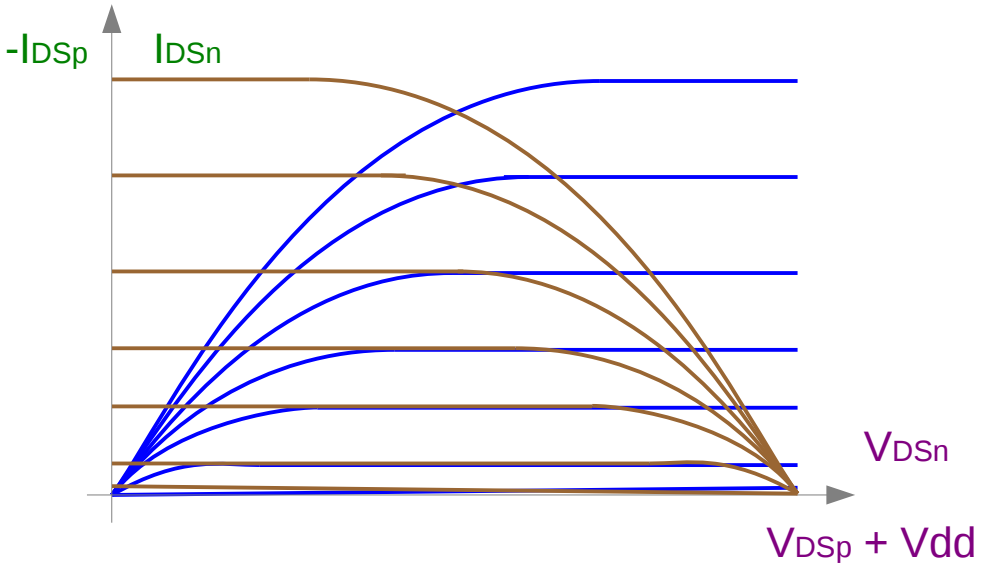


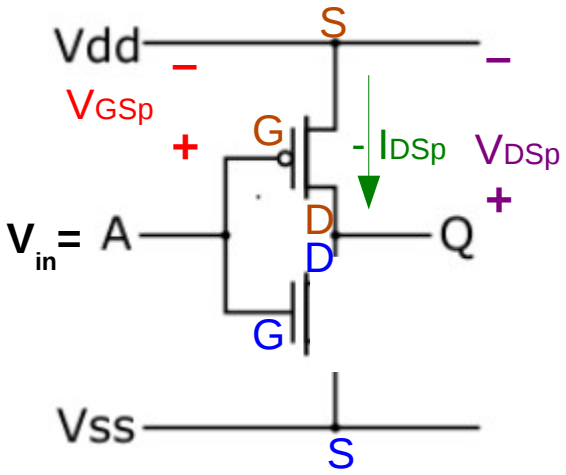
Overlay pMOS & nMOS curves

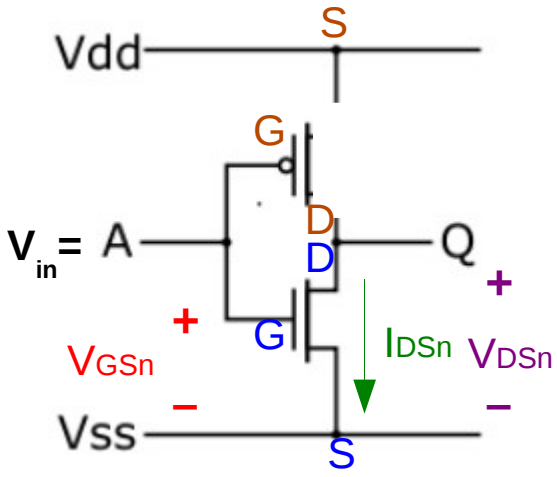
https://en.wikipedia.org/wiki/CMOS

$$V_{in} = V_{GSp} + V_{dd} = V_{GSn}$$

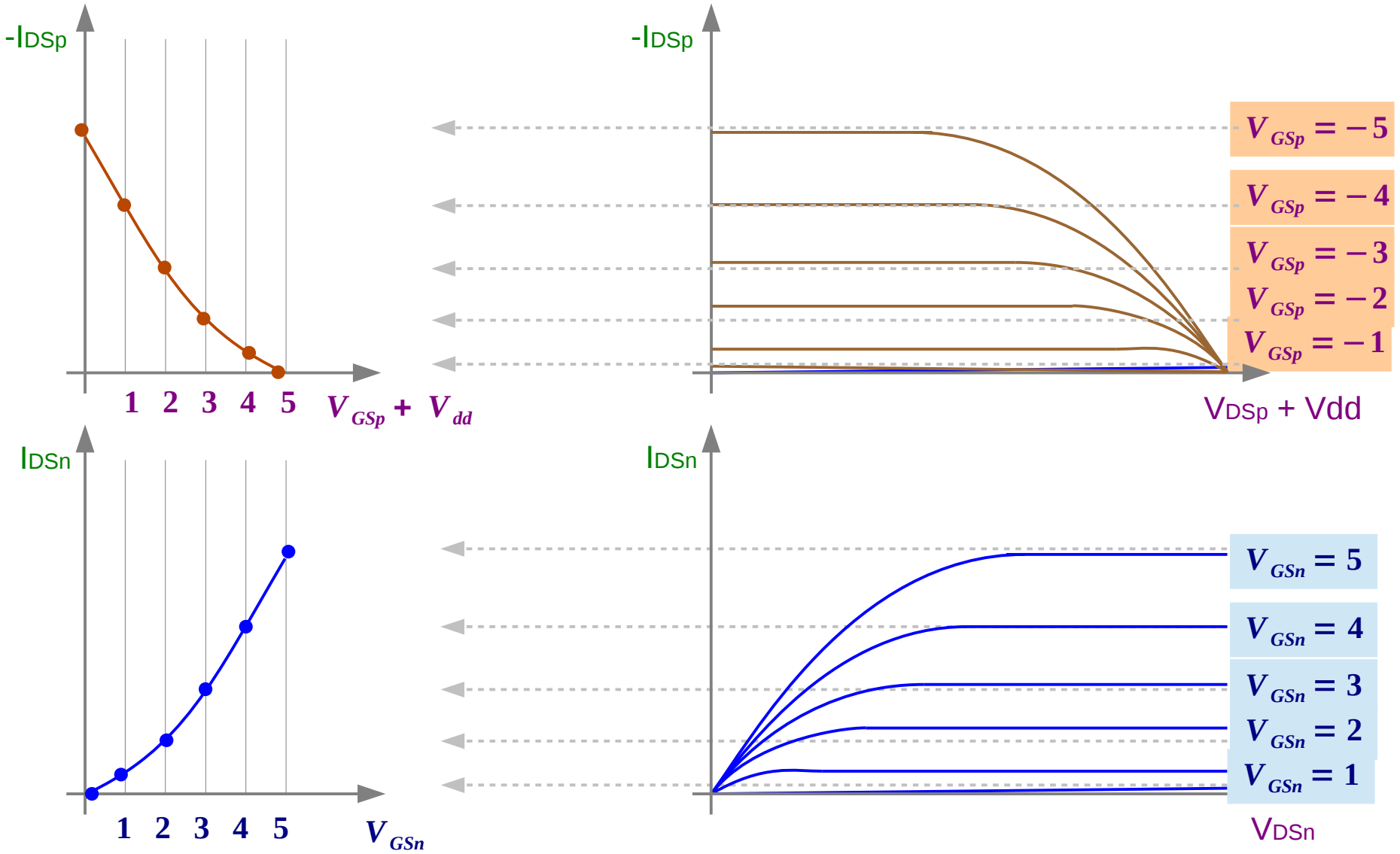
$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$







[Ids–Vgs], [Ids–Vds] Characteristic Curves

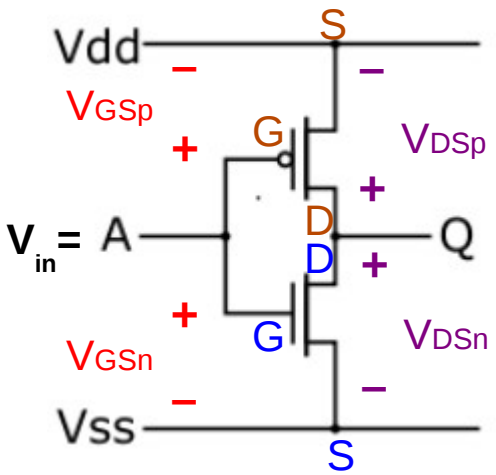


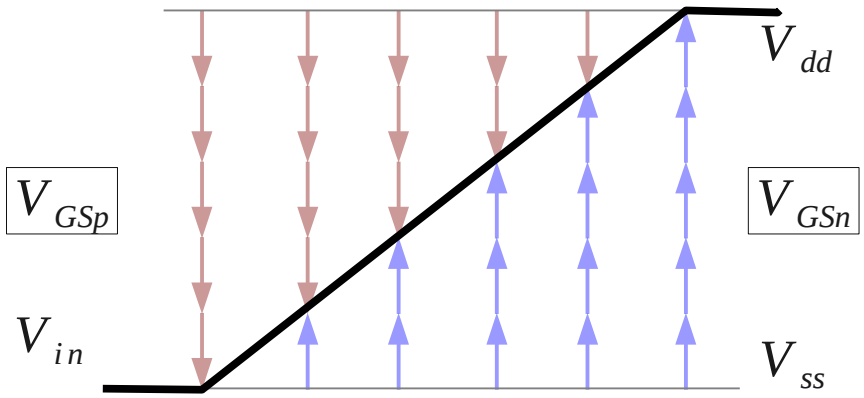
Vin : L → H

$$V_{in} = V_{GSp} + V_{dd} = V_{GSn} \quad \bigstar$$

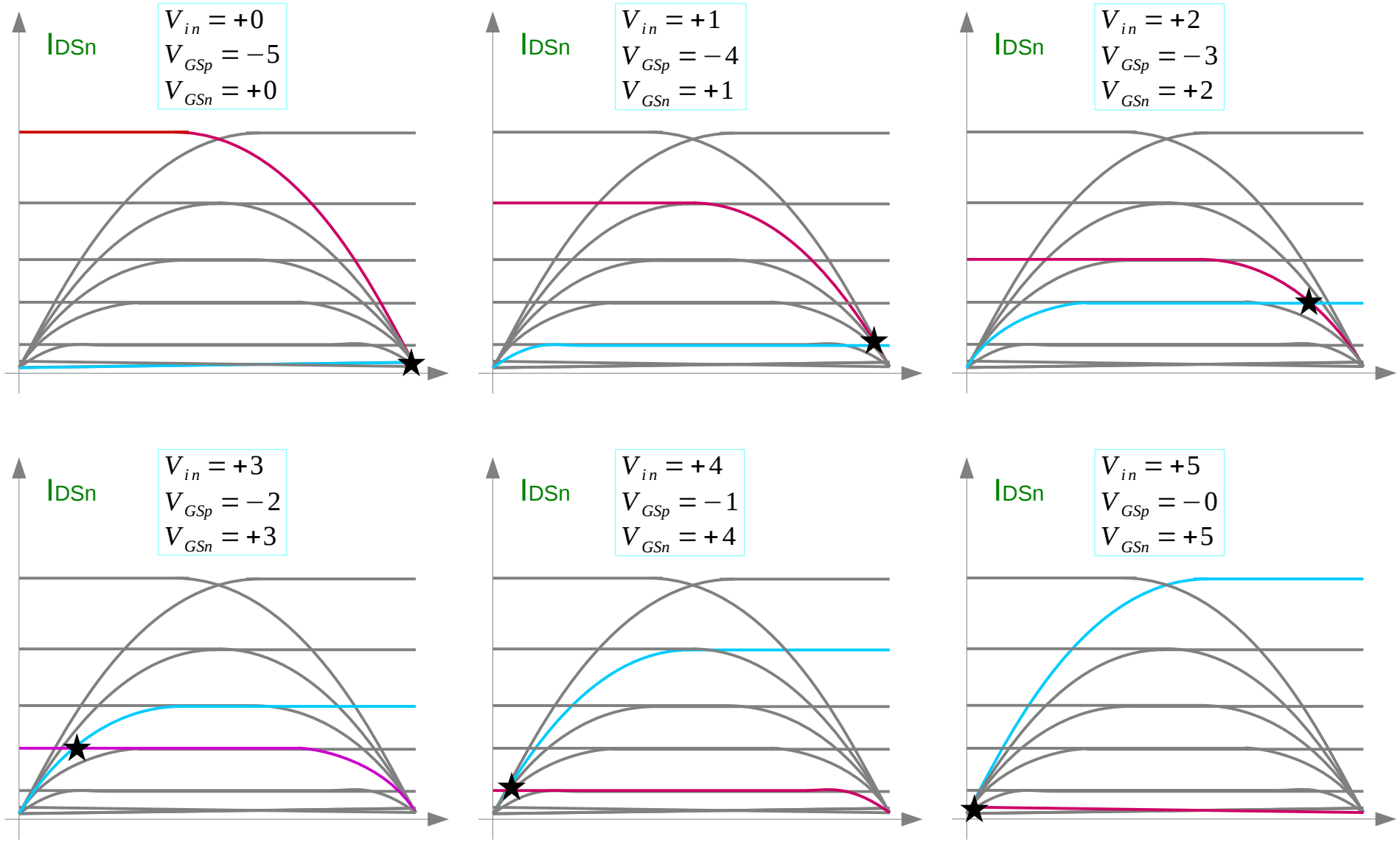
$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

V_{in}	0	1	2	3	4	5
V_{GSp}	-5	-4	-3	-2	-1	0
V_{GSn}	0	1	2	3	4	5

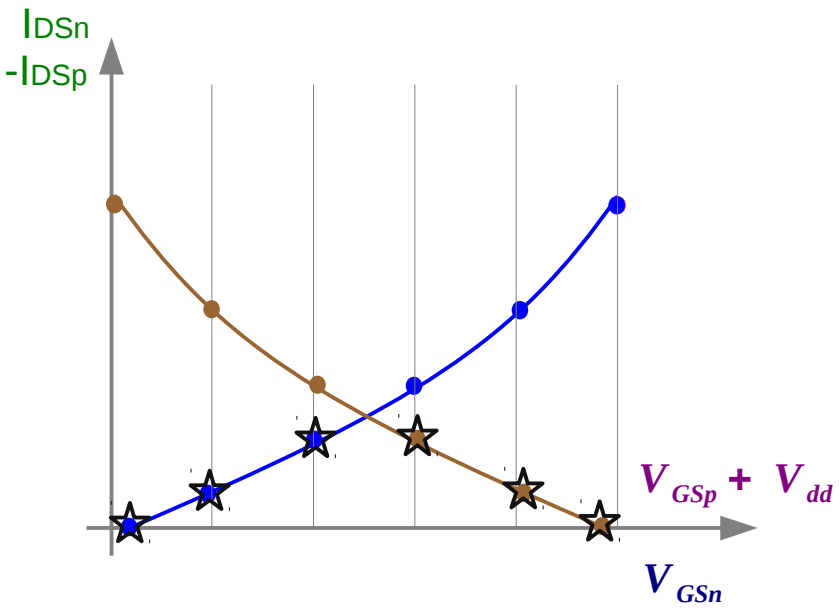


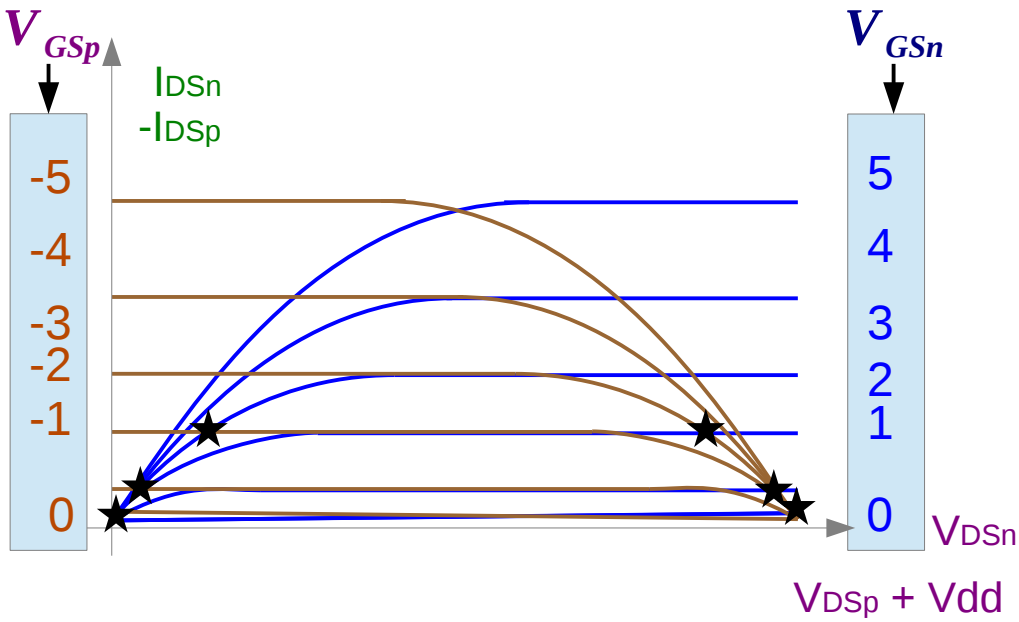


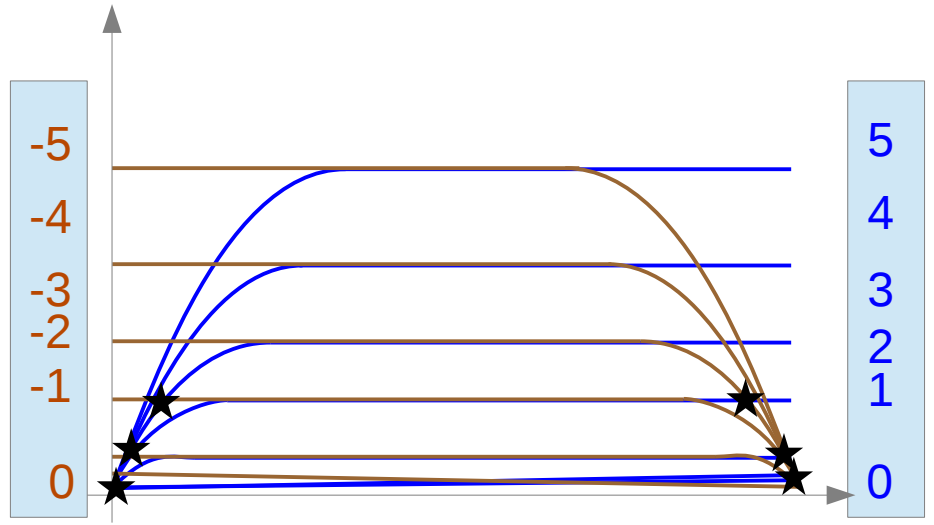
Intersect Points



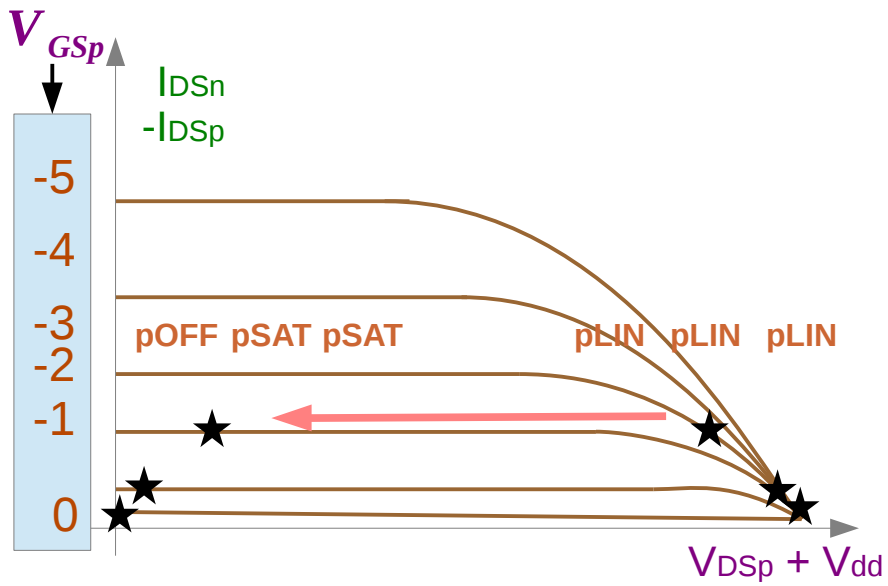
Intersect Points in [Ids–Vgs], [Ids–Vds] Curves

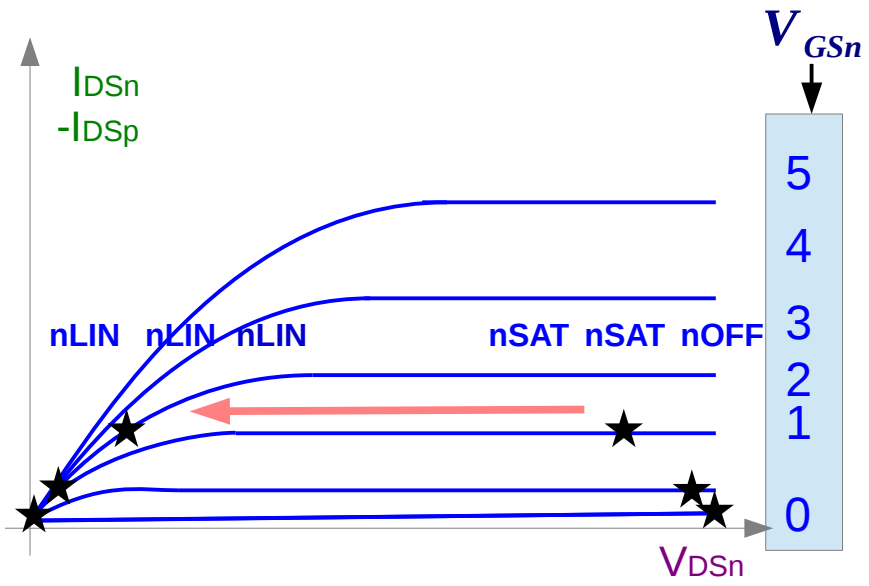






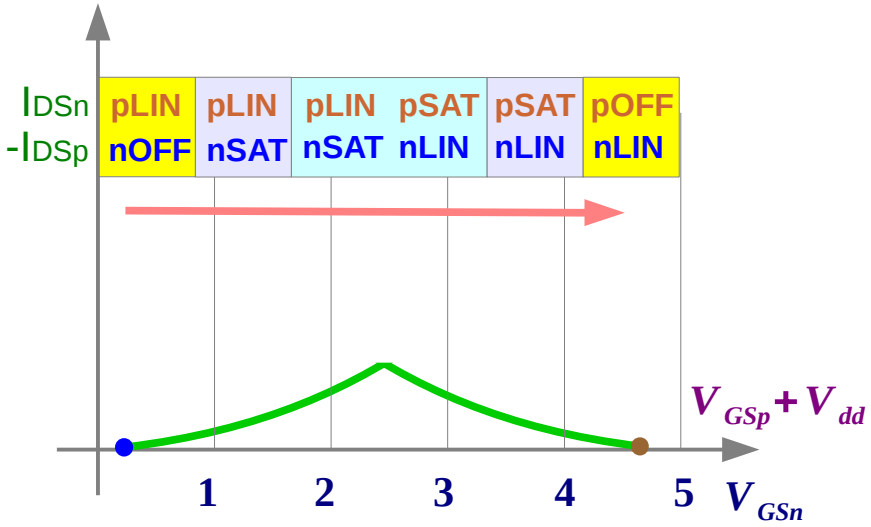
Mode Changes



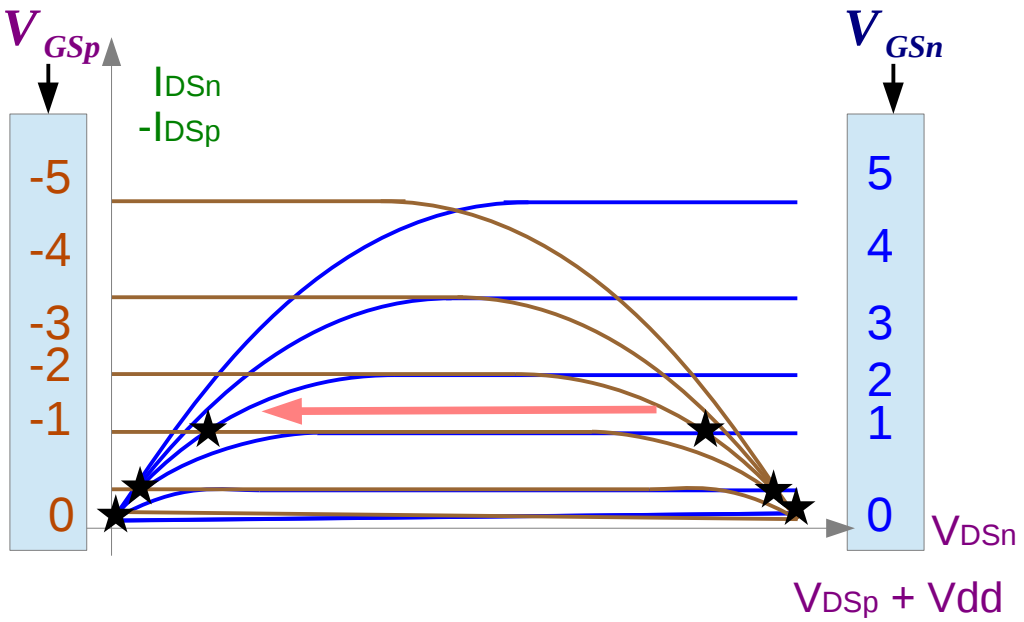


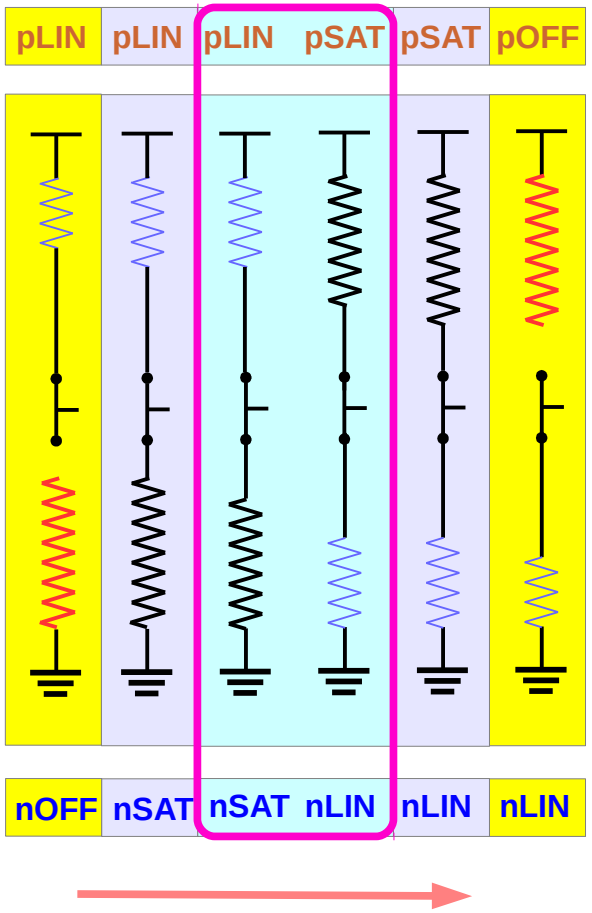
V_{in}	0	1	2	3	4	5
V_{GSp}	-5	-4	-3	-2	-1	0
V_{GSn}	0	1	2	3	4	5

pLIN nOFF	pLIN nSAT	pLIN nSAT	pSAT nLIN	pSAT nLIN	pOFF nLIN

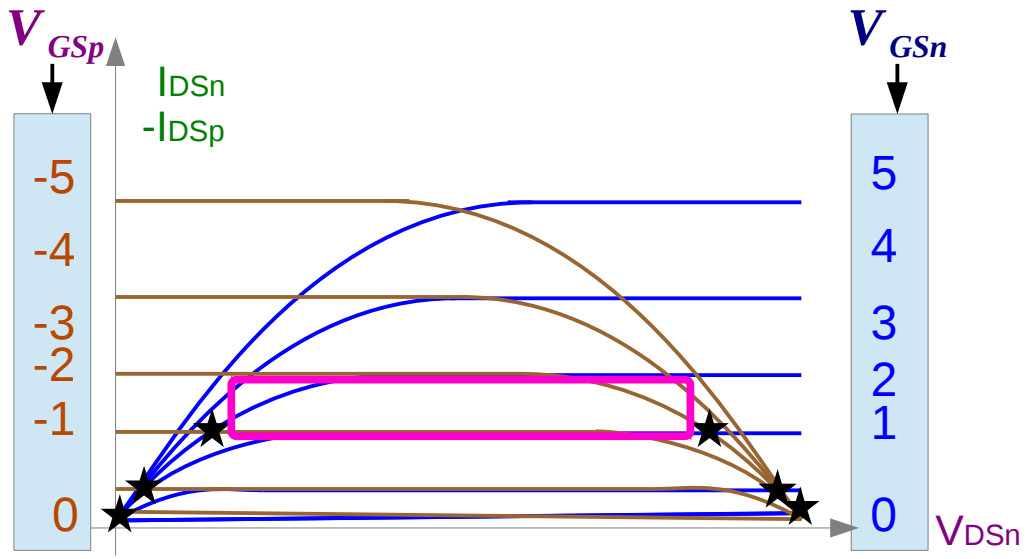


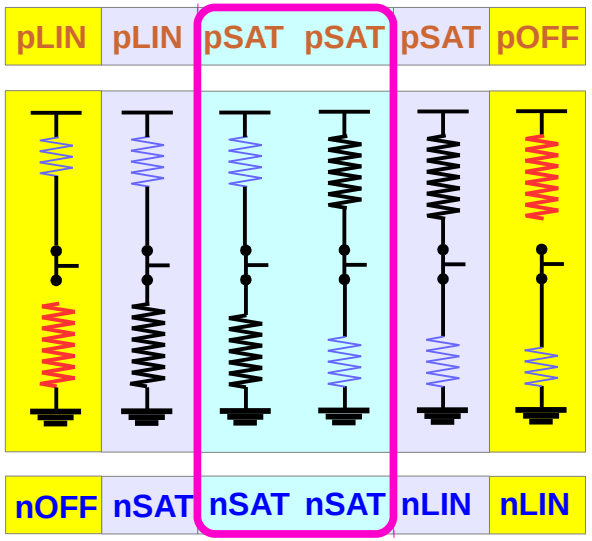
Resistance and Mode Changes

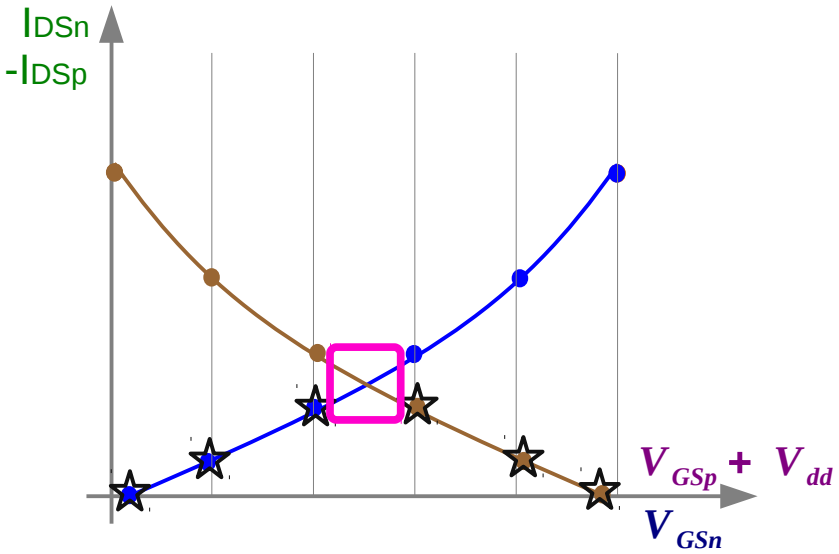


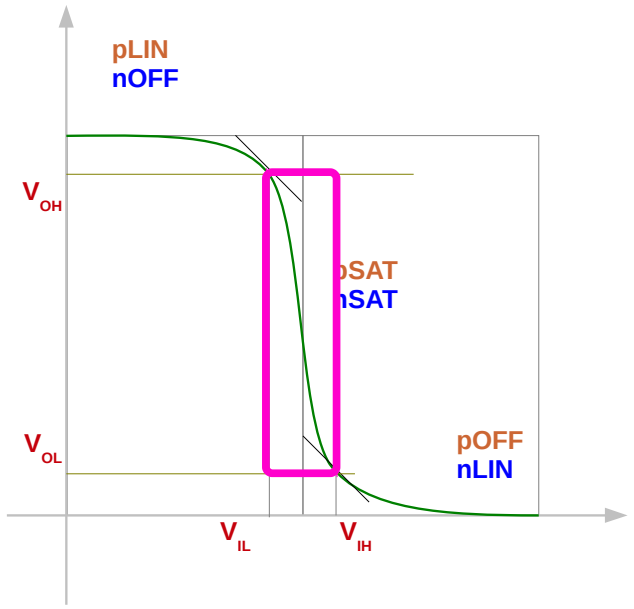


Abruptly Changing Region

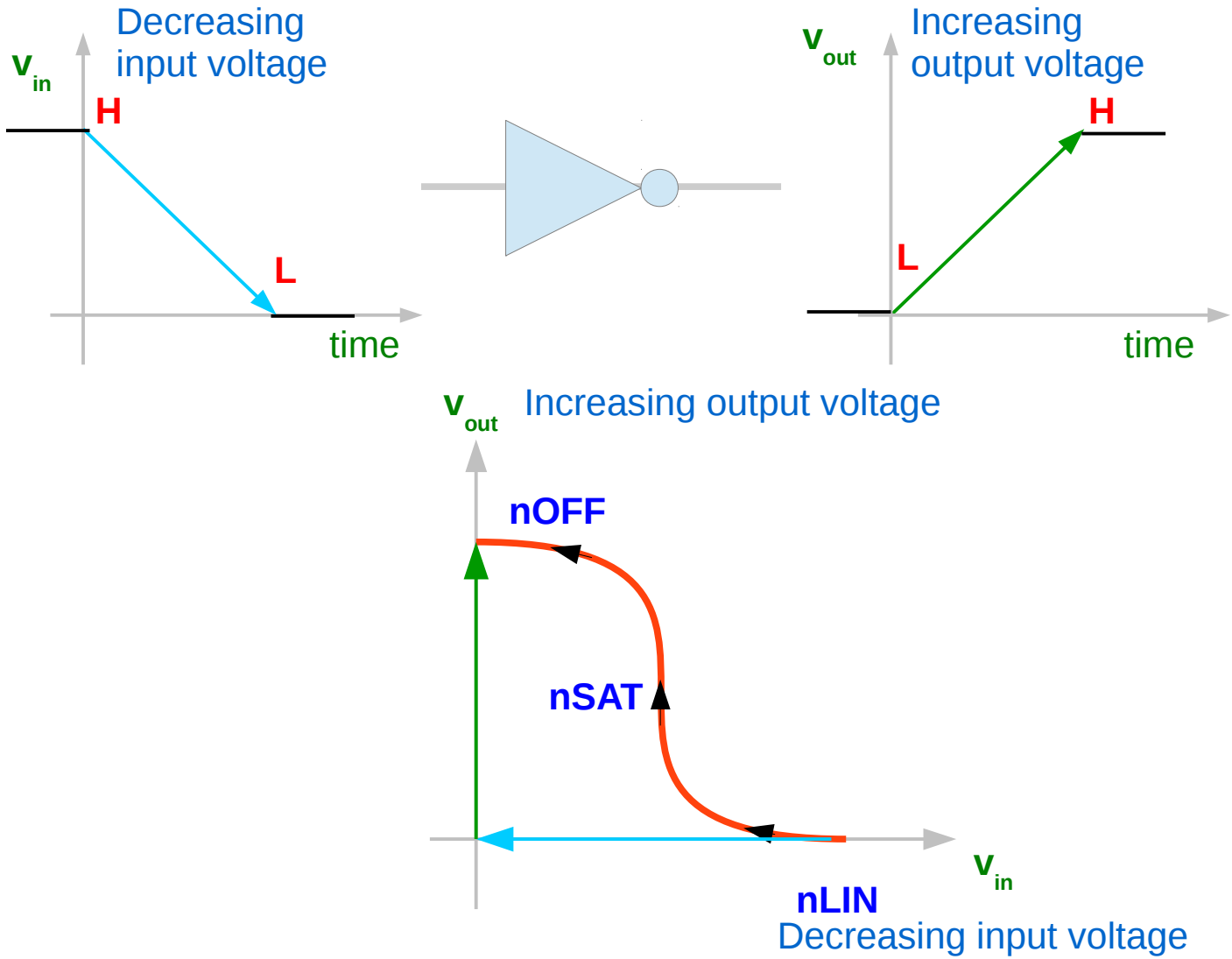




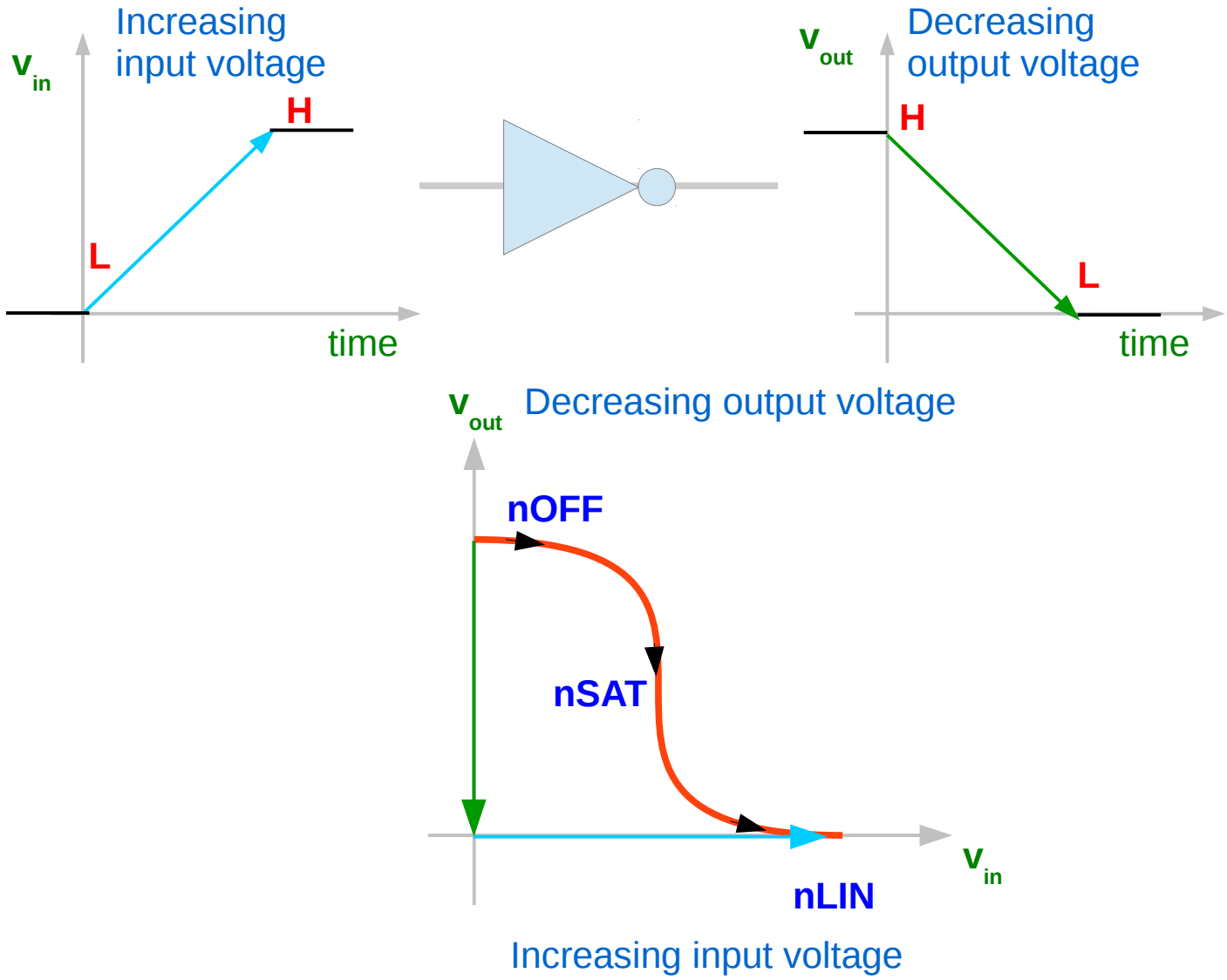




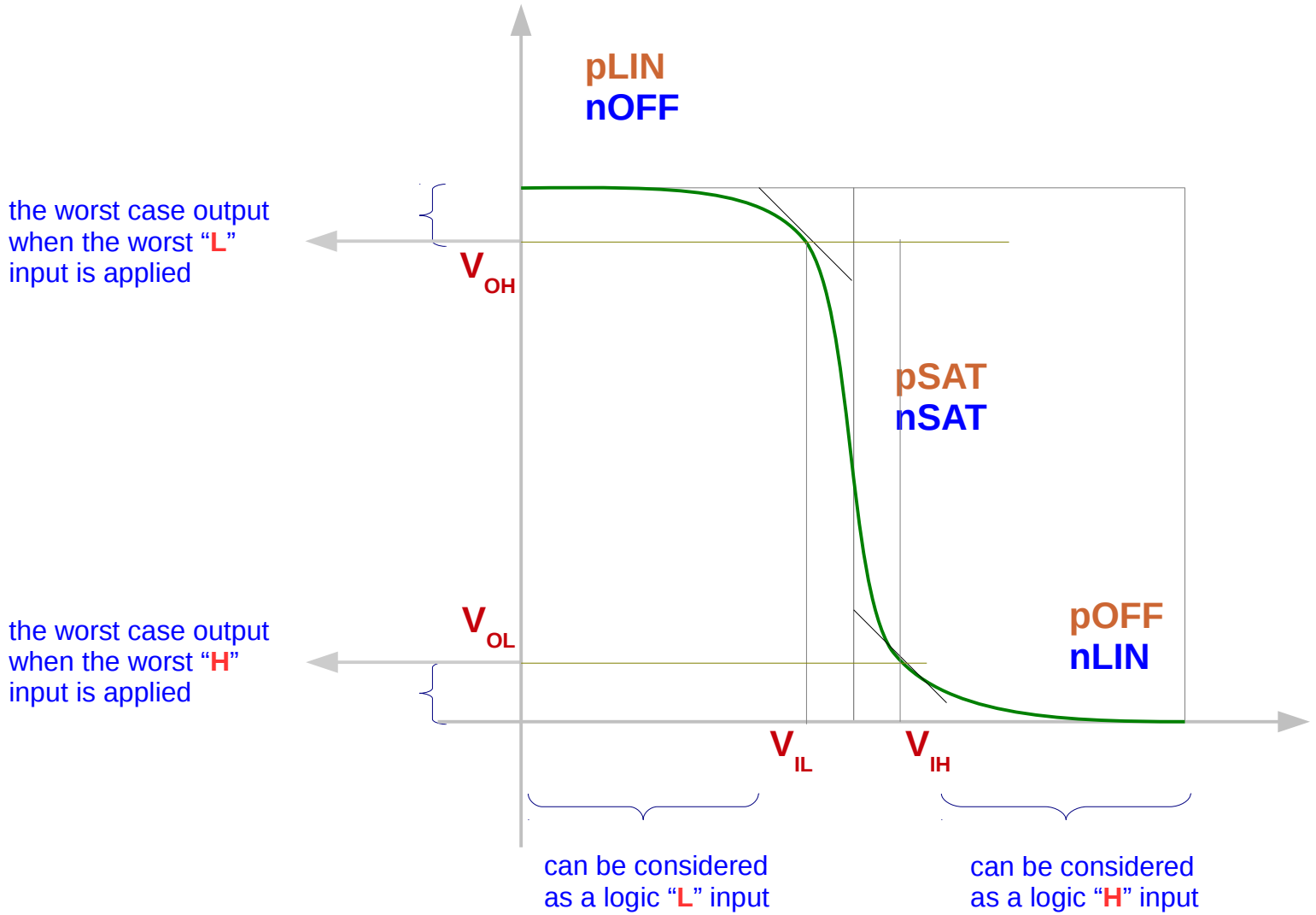
Input Switching 1 → 0



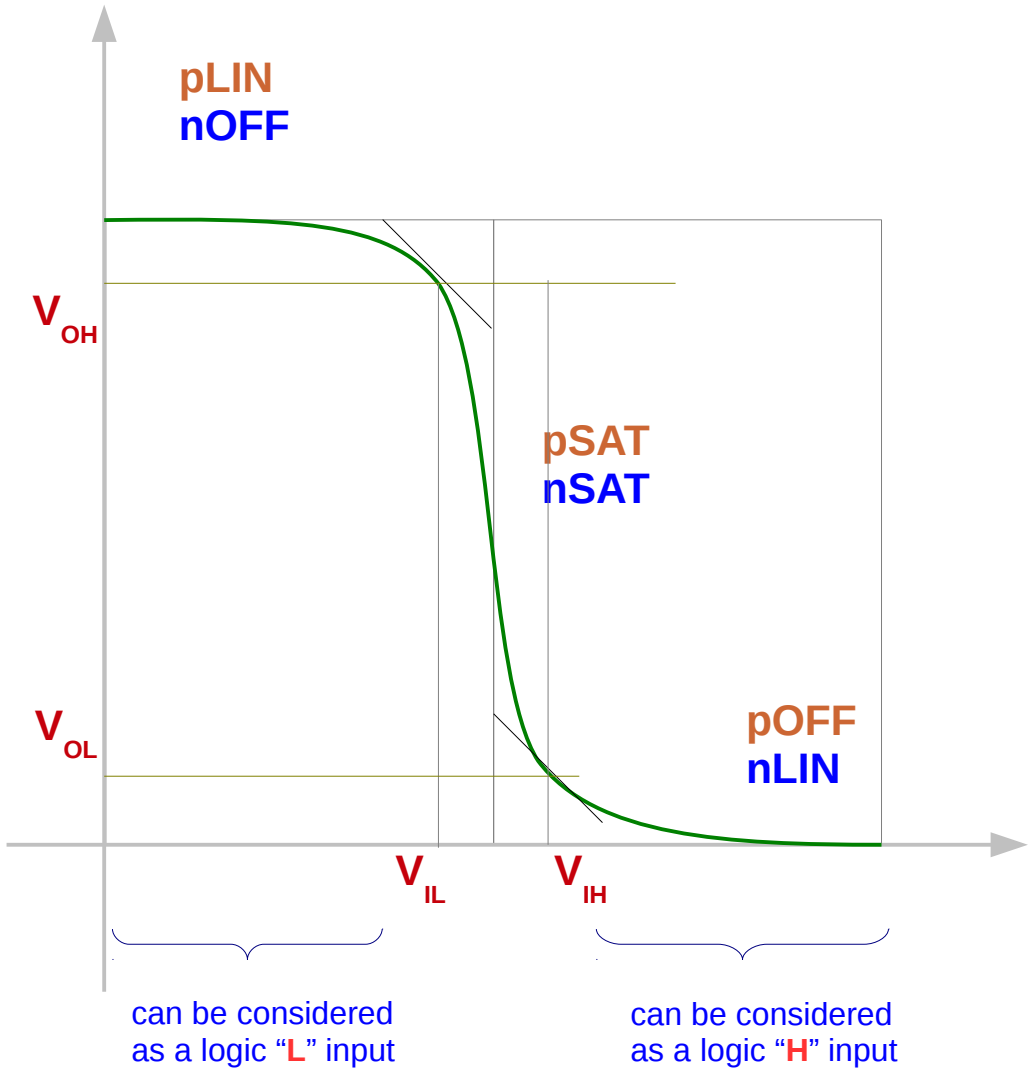
Input Switching 0 → 1

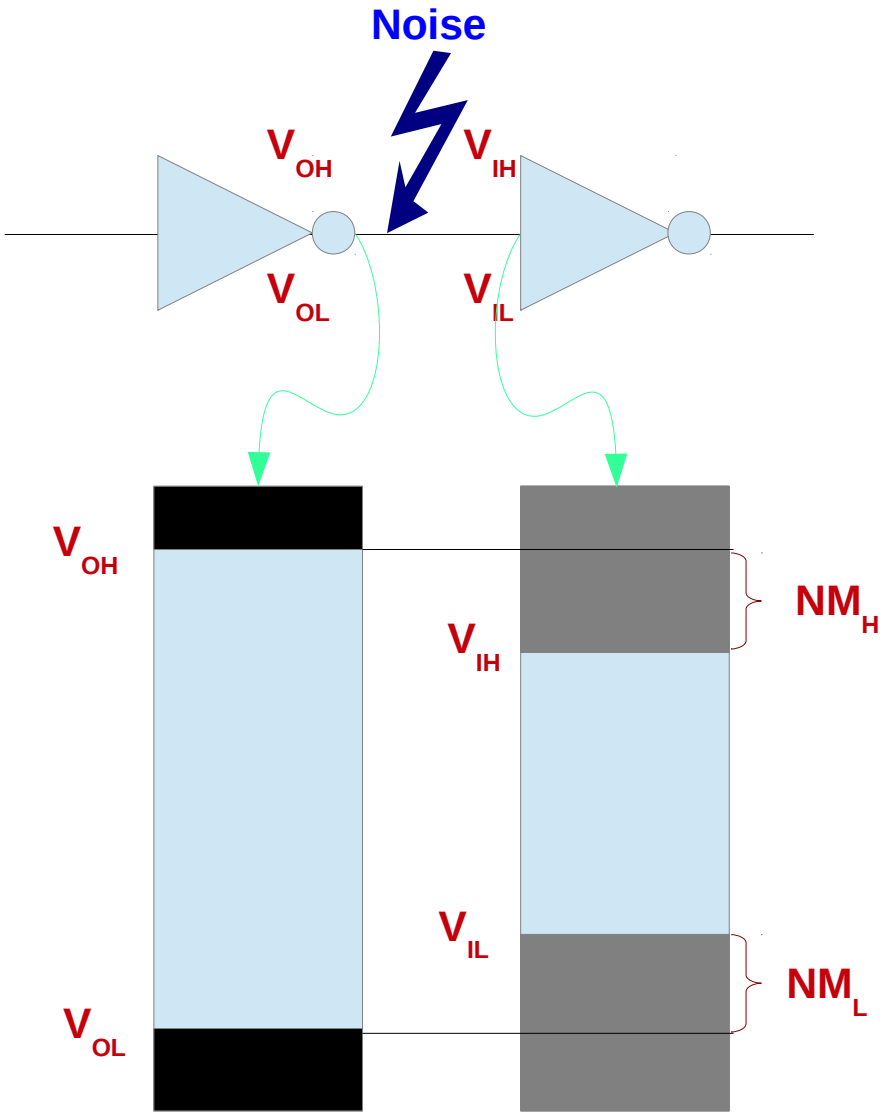


[V_{IL}, V_{IH}] & [V_{OL}, V_{OH}]



Noise Margin





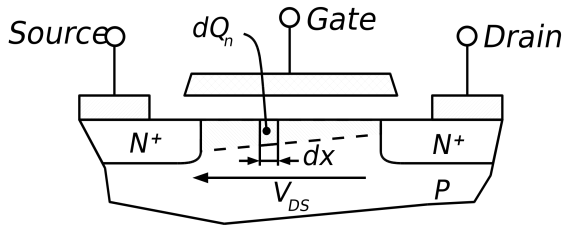
Simple Transistor Model

https://en.wikipedia.org/wiki/CMOS

Cutoff, subthreshold, or weak-inversion mode

When $V_{GS} < V_t$:

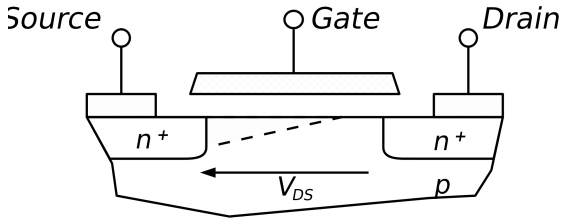
$$I_d = 0$$



Triode mode or linear region (the ohmic mode)

When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

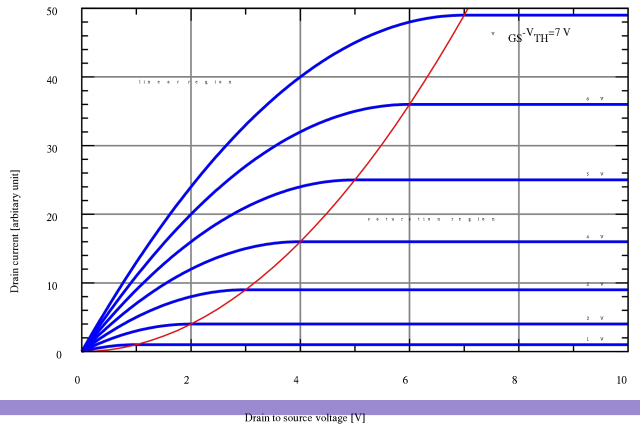
$$I_d = k' \frac{W}{L} \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$



Saturation or active mode

When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$

$$I_d = \frac{1}{2} k' \frac{W}{L} (v_{gs} - v_t)^2$$



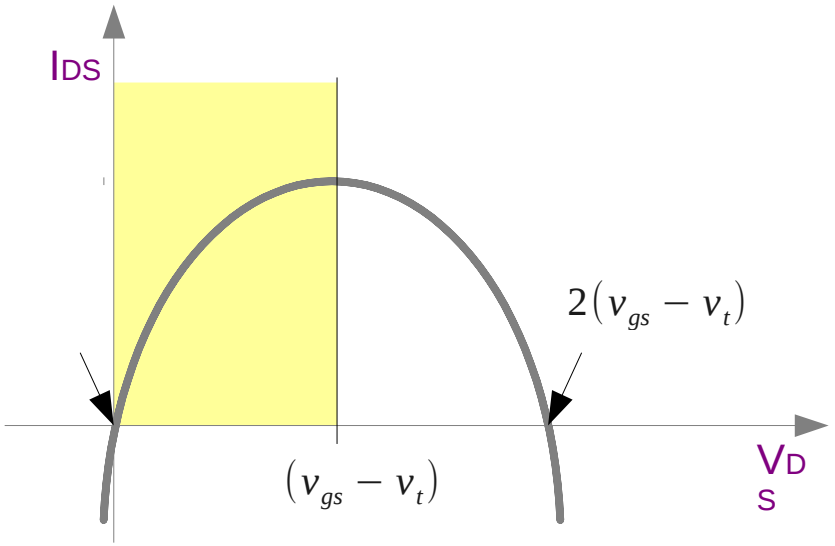
Linear and Saturation Models

https://en.wikipedia.org/wiki/CMOS

linear region

When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

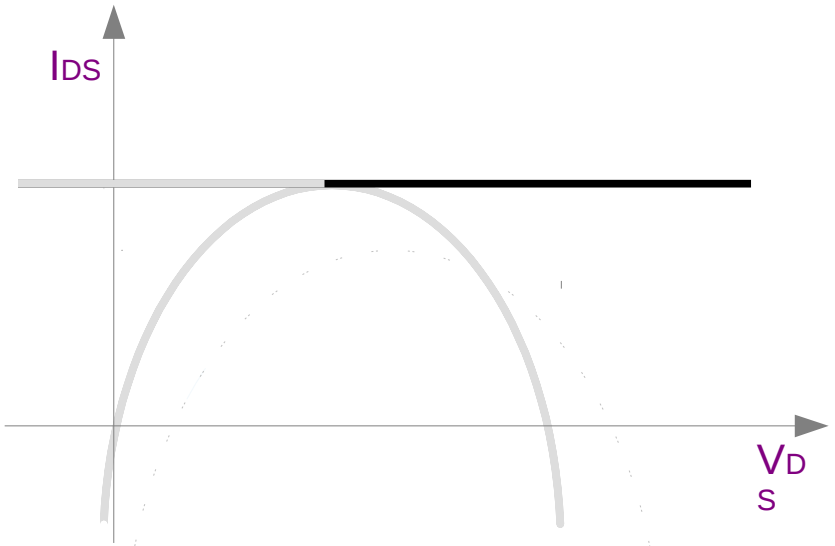
$$I_d = k' \frac{W}{L}\left[(v_{gs} - v_t)v_{ds} - \frac{1}{2}v_{ds}^2\right]$$



Saturation or active mode

When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$

$$I_d = \frac{1}{2}k' \frac{W}{L}(v_{gs} - v_t)^2$$



Bias Conditions

https://en.wikipedia.org/wiki/CMOS

Cutoff

$V_{GS} < V_t$:

Linear region

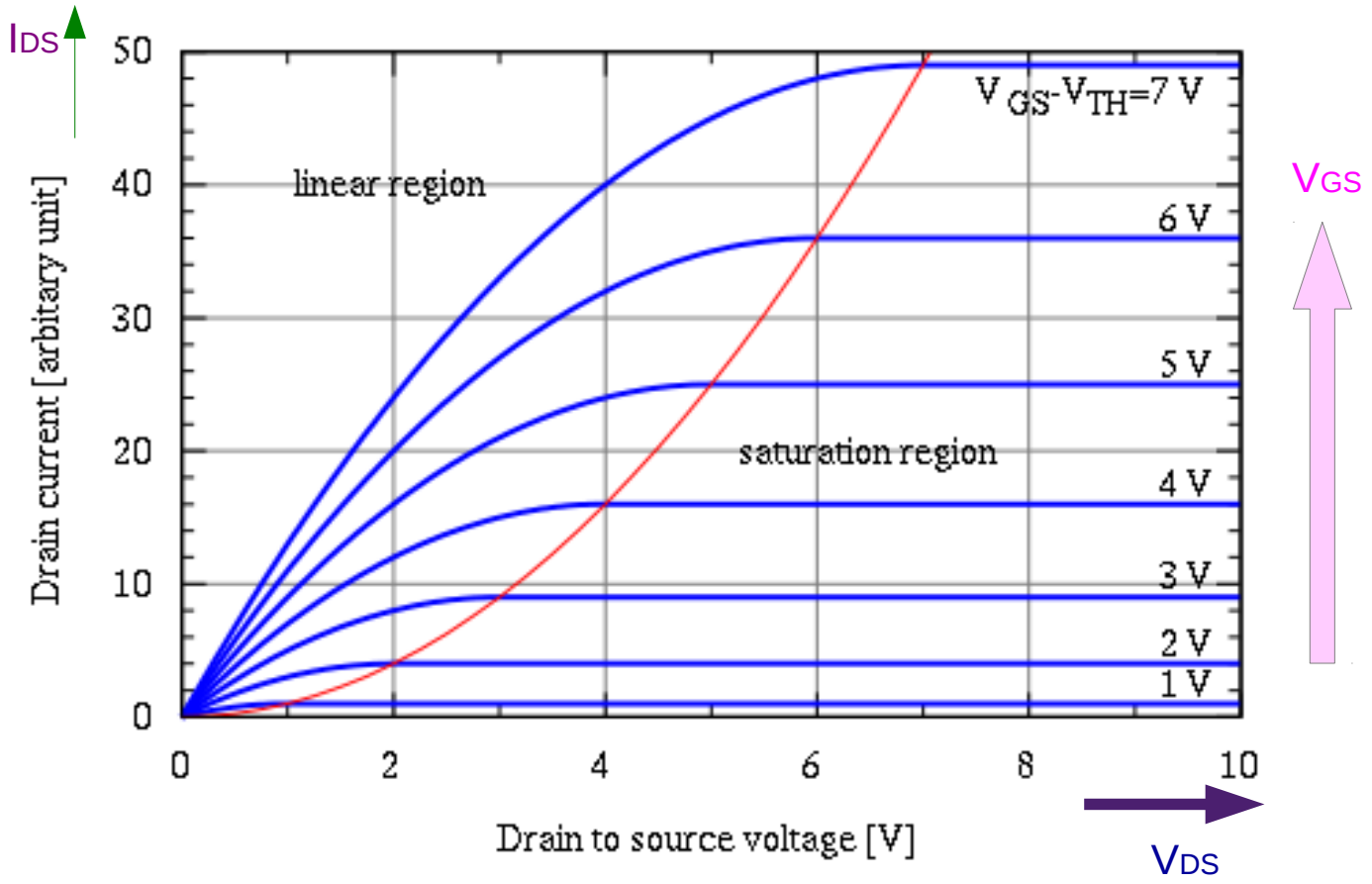
$V_{GS} > V_t$

$V_{DS} < (V_{GS} - V_t)$

Saturation

$V_{GS} > V_t$

$V_{DS} > (V_{GS} - V_t)$



Characteristic Curve

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[11] https://en.wikiversity.org/wiki/Verilog_programming_in_plain_view